

**PERFORMANCE ANALYSIS OF 20 NM SI AND GE CHANNEL BASED PENTAGONAL AND TRAPEZOIDAL NWT**

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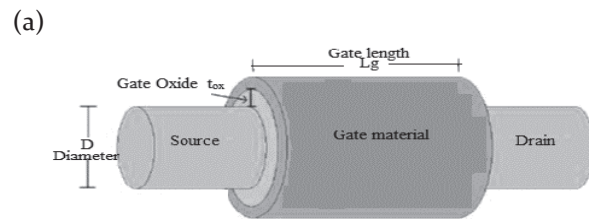
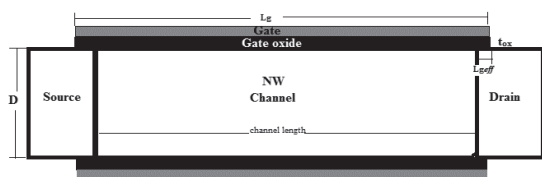
**Abstract:** In this paper, we have investigated the variability in the performance of GAA FET (Gate All Around Field Effect Transistor) due to their cross section shapes and channel materials with the aid of 3D TCAD simulations. Pentagonal and trapezoidal Cross section shapes have been designed for constant diameter and height (10nm) with doped Si and Ge channel. The performance is evaluated in terms of Ion current, leakage current, switching speed, transfer and output characteristics, Drain Induced Barrier Lowering (DIBL), Subthreshold Swing (SS), threshold voltage (Vti) and compared with triangular NWT. After comparison, it shows that Si Pentagonal NWT structure is showing better performance i.e. high on-current, low DIBL and Low SS. Ge NWT offer better leakage current.

**Keywords:** GAA FET, TCAD, NWT, DIBL, SS, Vti etc.

**Introduction:** With the shrinkage in technology, transistor density is increasing. Therefore, downscaling of transistors is required. But making transistors smaller leads to degradation in device performance [1]. This degradation is due to dominant short channel effects (SCEs) such as drain induced barrier lowering (DIBL), subthreshold swing (SS), threshold voltage (Vti) etc. Several structures like double gate [2], tri-gate transistors [3] have replaced MOSFETs. After tri-gate, gate all around structures have the advantages of strong electrostatic control of channel by gate [4]. The circular, rectangular and triangular NWTs (TNWT) have been discussed in the literature [5].

Semiconductor NWs are emerged as a powerful materials that can be used in controlled growth and organizations [6], which is making it an evolutionary technology of nano scaled electronics and photonic devices. Inorganic NWs have a higher conducting and higher electrical properties. A NW structure is an object with 1D aspect in which the length to width ratio is greater than 10 and possible width is less than 10 nm. NWs have smallest dimension for efficient exciton and transport of electrons. Electrical conductivity of NW is also affected by structural defect, reduces impurity and its dimensions like cross sectional area, corner effects etc.

**GAA NWFET:** GAA NWFETs are allowed to sustain the relentless progress in CMOS scaling. NWFETs can be formed in high yield with reproducible and repeated electronics properties as required for CMOS technology [7]. Second, the channel diameter can be prepared below 10nm without compromising its electric performance.



**Figure 1:** (a) Schematic 2D representation of GAA NWFET, (b) Schematic 3D representation of CNWFET.

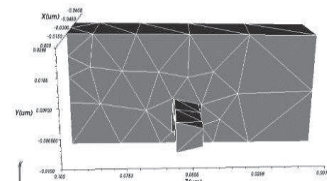
In addition, the smooth surface, crystalline structure and the ability of axial and radial NW hetrostructures can suppress the charge scattering [8].

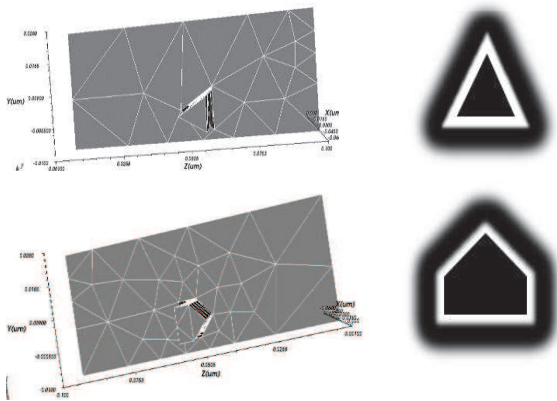
**Device design:** In this work, we have designed three different cross section shapes GAA NWT such as triangular [9], trapezoidal and pentagonal cross sections.

**Table I** Architecture parameters of device

Architecture Parameter	Value
Lambda Design Rule(nm)	10
Structure orientation	<100>
Channel Height (nm)	10
Channel Diameter (nm)	10
Gate oxide(nm)	1
Channel length(nm)	20
Substrate doping (cm <sup>-3</sup> )	2e17
Source/drain doping (cm <sup>-3</sup> )	2.063e20
Channel doping(cm <sup>-3</sup> )	1e15

Tungsten W (4.5eV) is used for gate terminal, source, drain, metal contacts, HfO2 (k = 20-25) is used as gate oxide to isolate the channel from gate.



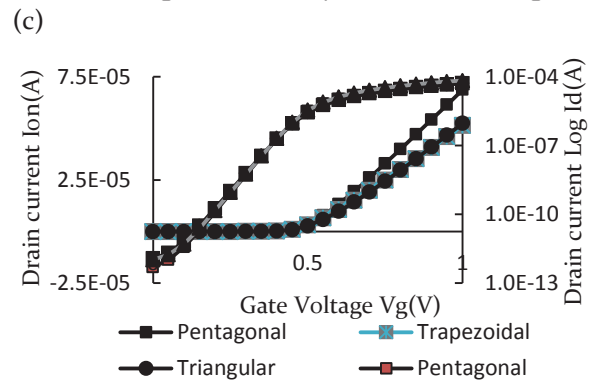
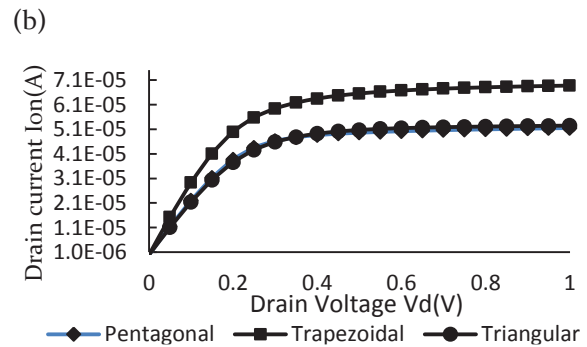
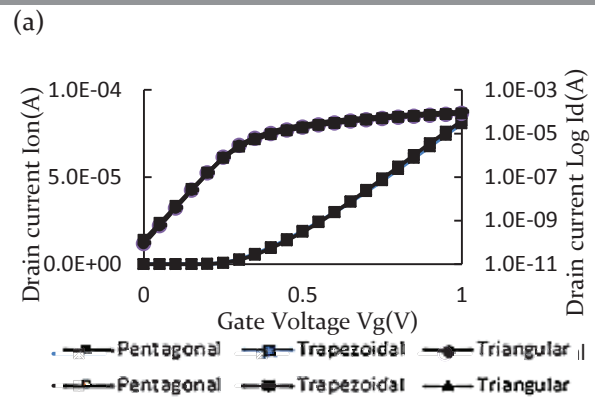
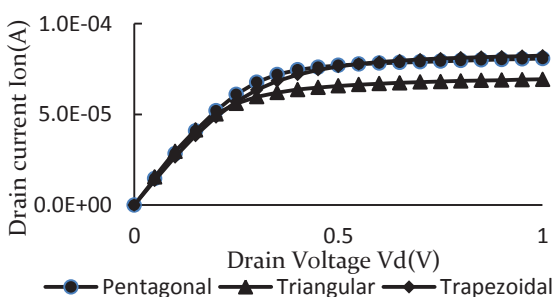


**Figure 2:** Schematic representation of 3-D perspective view and 2-D cross sections.

Two different channel materials Si and Ge are used and a comparative analysis has been done for these devices [10]. The device is designed for different height with a constant channel width 10nm and for different width taking constant height 10nm respectively. Remaining all parameter are common for all devices. Figure2 shows a 3-D perspective view and 2-D cross section of the channel region of the GAA NWFET. The 3D device structure simulated with Visual TCAD.

**Device Simulations and analysis:** The designed device has been simulated with concentrations given in table 1 at 300k using the classical drift-diffusion approach. All simulations have been done with a range of drain voltage from  $V_d = 0.05-1V$ . The Threshold voltage ( $V_{ti}$ ) for all designed NWTs have been extracted from transfer characteristics in active region with drain voltage  $V_d = 0.05V$ .  $I_{off}$  current is taken at  $V_g = 0V$  and drive current ( $I_{on}$ ) is taken at  $V_g = 1V$  with constant drain voltage  $V_d = 0.5V$ . The DIBL parameter is obtained as the horizontal displacement of I-V characteristics at drain current of  $1.0e-7 A$  and constant drain voltage  $V_{lin} = 0.05V$  and  $V_{sat} = 1.0V$ . The subthreshold swing is obtained from transfer characteristics.

**Figure 3:** (a) Output characteristics plot of SiNWT with different cross sectional shapes (b) Transfer characteristics SiNWT (c) Output characteristics of GeNWT (d) Transfer characteristics of GeNWT.



The output characteristics of GAA NWFET devices have been extracted with varying drain voltage (0-1.0V) at constant gate voltage  $V_{gs} = 1.0V$ . The transfer characteristics of GAA NWFET devices have been extracted with varying gate voltage on constant drain voltage  $V_{ds} = 1.0V$ .

Figure 3 show the relation of  $I_d-V_d$  and  $I_d-V_g$  of devices. Figure 3(a) and (c) depict that the drain current is directly proportional to the drain voltage in linear region. Further  $I_d$  gets saturated w.r.t  $V_d$  and it is called saturation region. Trapezoidal NWT (TrNWT) has maximum  $I_{on}$  current as compared to TNWT and Pentagonal NWT (PNWT) because  $I_{on}$  current is directly proportional to cross sectional area. Device with higher cross section area has more conducting area and more charge carriers. TNWT has minimum cross section area thus it shows the minimum  $I_{on}$  current. Figure 3(b) and (d) showed the transfer characteristics of SiNWT and GeNWT

with different cross sectional areas. Id-Vg plot shows that SiNWT has small Vti than GeNWT.

Figure 4(a) shows the TrNWT with Si channel has maximum Ion Current (6.5e-05). Si has higher DoS as compared to Ge so it shows higher Ion current in short channel designed devices. Figure 4(b) shows the off current of different devices. Off current is a kind of leakage current which flows in the device when voltage is not applied. Ge channel devices have better leakage current than Si channel devices. Figure 4(c) shows the Ion/Ioff ratio of different devices. Ion/Ioff presents the switching speed of devices and it is approximately anti-proportional to the cross section area.

TNWT with Ge channel shows the maximum Ion/Ioff ratio (7.43E07) as compared to other devices. Figure 4(d) depicts the SS of GAANWT devices. The minimum value of SS shows the leakages and lower SCEs.

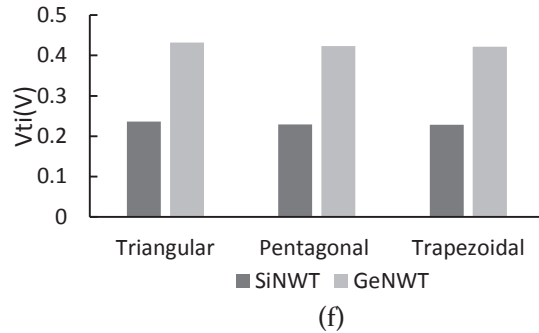
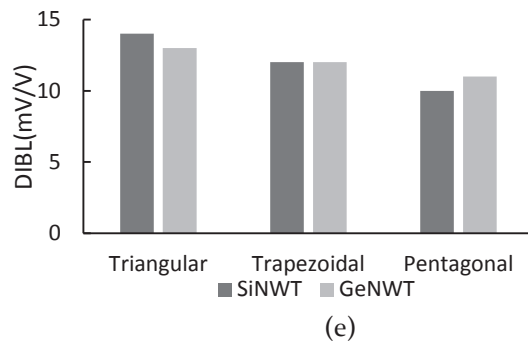
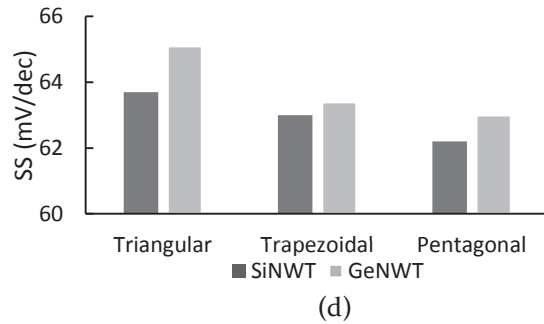
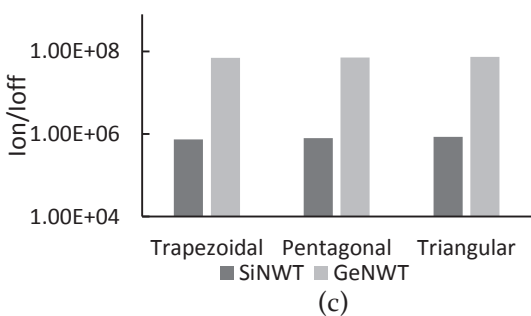
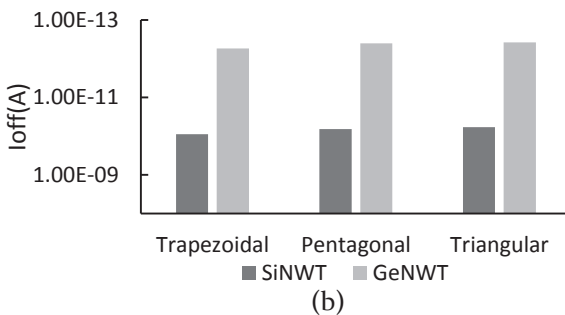
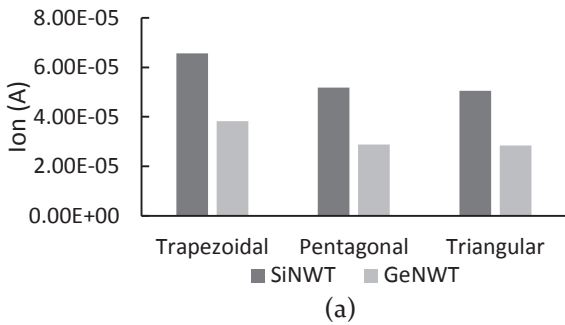


Figure 4 a comparative analysis of(a) Ion current of SiNWT and GeNWT, (b ) Ioff current of SiNWT and GeNWT (c) Ion/Ioff ratio of SiNWT and GeNWT.(d) SS of SiNWT and GeNWT, (e) DIBL of SiNWT and GeNWT and (f) Vti of SiNWT and GeNWT.

Basically SS effects depend upon corner effect, channel length and gate control ability. Thus SiPNWT has minimum SS (62.2mV/dec) and GeTNWT has maximum SS (65.3mV/V). Figure 4(e) shows the DIBL of GAANWT. SiPNWT has minimum DIBL (10mV/V) and SiTrNWT has maximum DIBL (14mV/V).

Figure 4(f) shows the Vti characteristics of GAANWT. Threshold voltage defines the voltage at which the device starts working. Basically short channel devices is used in low power applications and need to have lower threshold voltage. So Si TNWT has maximum Vti (0.2386V) and TrNWT has minimum Vti (0.2285V). Si PNWT Vti (0.2294V) lies in between TNWT and TrNWT. The same relations are hold by GeNWT. Ge TrNWT has minimum Vti (0.4217V).

Table II Simulated results of GAANWT with different cross section shapes and channel materials

**Table II** presents the effects of cross sections shapes and channel materials on Ion and Ion/Ioff ratio of NWT

Cross Section Shape	SS(mV/de c)		DIBL(m V/V)		Vti(V)	
	Si	Ge	Si	Ge	Si	Ge
TNWT	63.7	65.1	14	13	0.2366	0.4317
PNWT	63	63.4	12	12	0.2294	0.4228
TrNWT	62.2	63	10	11	0.2285	0.4217

**Table III** Simulated results of GAANWT with different cross section shapes and channel materials

Cross Section Shape	Ion(A)		Ioff (A)		Ion/Ioff	
	Si	Ge	Si	Ge	Si	Ge
TNWT	5.05E-05	2.84E-05	5.9E-11	3.82E-13	8.54E05	7.43E07
PNWT	5.18E-05	2.88E-05	6.5E-11	4.02E-13	7.8E05	7.16E07
TrNWT	6.57E-05	3.83E-05	8.8E-11	5.47E-13	7.4E05	7.0E07

**Table IV** Comparison between different cross section shapes and channel materials

Parameter		PNWT vs TNWT / TrNWT	Triangular [5]
Ion	Si	+2.89 % than TNWT -21% than TrNWT	+5 times
	Ge	+1.40% than TNWT -24% than TrNWT	+3 times
Ion/Ioff	Si	-7.50% than TNWT +6.04% than TrNWT	-4 times
	Ge	-3.63% than TNWT +2.28% than TrNWT	17 times
SS	Si	-2.35% than TNWT	-0.49%

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		-1.26% than TrNWT	
	Ge	-3.22% than TNWT -0.63% than TrNWT	-1.56%
DIBL	Si	-28% than TNWT -16% than TrNWT	same
	Ge	-15% than TNWT -8.33% than TrNWT	-21%
Vti	Si	-3.04% than TNWT +0.39% than TrNWT	-26%
	Ge	-2.06% than TNWT +0.26% than TrNWT	+36.38%

Table III shows the variation of SCEs with variation of channel materials and shapes. Table IV presents the Comparison between different cross sections and channel materials. Si TrNWTs have shown maximum Ion current because of maximum conducting area. But due to losses of gate controllability, it has maximum SCEs.

**Conclusion:** It was found that PNWT can improve the electrical results. PNWTs have better performance in terms of SCEs like SS and DIBL and optimum Ion/Ioff ratio, whereas Si Trapezoidal NWTs have shown maximum Ion current because of maximum conducting area. But due to losses of gate controllability, it has maximum SCEs. Triangular NWT has good controllability due to the corner effects so it has less SCEs than TrNWTs but due to small cross section area it has minimum Ion current. In this work, Silicon NWTs have better Ion and better SCEs than Ge. But Ge has shown better ion/Ioff Ratio and better leakage current.

**Acknowledgment:** I am highly grateful to Dr. M. S. Saini, the Director, Guru Nanak Dev Engineering College (GNDEC), Ludhiana, for providing this opportunity to carry out the present work. The constant guidance and encouragement and access to facilities received from the Faculty and staff of Department of Electronics & Communication Engineering, GNDEC, Ludhiana, have been of great help in carrying the present work and is acknowledged with reverential thanks.

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